Problem #1

What is needed here is a 3 bit counter that can be synchronously reset after the count reaches 5, so that it will count from 0-5. To go with that we may need some logic to recognize a pattern on the Qs to produce the desired output waveform.

In the description that follows, D is the output of the recognition Decision. It is a signal that will be high when it is time to reset the state to 000.

Q_0 should toggle except when D is low, in which case it should force a low output. Since a JK toggles when both inputs are high and forces a low when K is high & J is low, we can connect K_0 to +5, since it is always high and J_0 to D.

$J_0 = D \quad K_0 = 1 \ldots$

Q_1 should toggle when Q_0 is high and D is high and force a low when D is low and hold when Q_0 is low.

	Q0	D	J1		Q0	D	K1
Toggle	1	1	1		1	1	1
Reset	X	0	0		X	0	1
Hold	0	1	0		0	1	0

$J_1 = Q_0 \cdot D \quad K_1 = (Q_0 \cdot D) + \overline{D}$

Q2 should toggle when Q0 & Q1 and D are all high. Hold when either Q0 or Q1 is low and D is high, and force a low whenever D is low

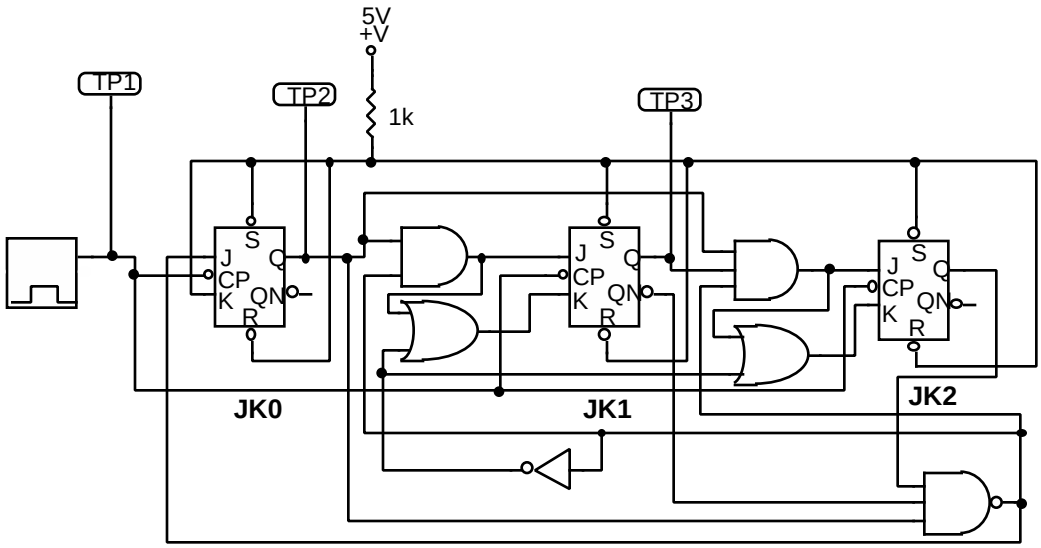
	Q0	Q1	D	J2		Q0	Q1	D	K2
Toggle	1	1	1	1		1	1	1	1
Reset	X	X	0	0		X	X	0	1
Hold	0	1	1	0		0	1	1	0
Hold	1	0	1	0		1	0	1	0

D \ Q_0Q_1	00	01	11	10
0	1	1	1	1
1	0	0	1	0

$J_2 = Q_0 \cdot Q_1 \cdot D \quad K_2 = (Q_0 \cdot Q_1) + \overline{D}$

To recognize the state of 5, combine $Q_0 \cdot \overline{Q_1} \cdot Q_2$ to form D.

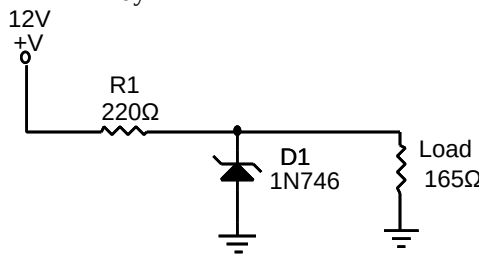
Q_1 will give the desired output waveform.



Problem #2

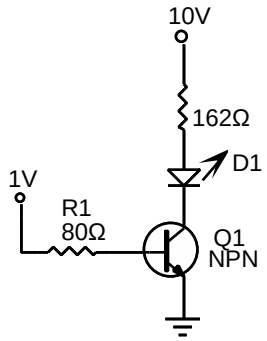
a) The first part of this problem is a resistor sizing exercise. The input is at 12V, the output will be at 3.3V, and the delta must be dropped across a resistor while supplying at least 25mA to a load. In preparation for part b, I chose to have 20mA flowing through the Zener, when the load was drawing 20mA. So a total of 40mA will be flowing through the resistor. $R = \frac{12V - 3.3V}{40mA} = \frac{8.7V}{40mA} = 217.5\Omega$. I chose the next larger standard size since it was closer to the desired value. There is no particular need to choose higher or lower in this case.

b) Since R_{dyn}=5Ω, the ΔV will simply be R_{dyn}*ΔI=5Ω*2mA=10mV



Problem #3

Since the signal provided to indicate activity is only 1V, and the voltage necessary to light the LED is 1.7V, we will need to use the 1V signal to control a higher voltage to actually energize the LED. The circuit below will do that, while delivering 50mA through the LED and maintaining the transistor in saturation because I into the base $= \frac{1V - 0.6V}{80\Omega} = \frac{0.4V}{80\Omega} = 5mA$



Problem #4

a) if Vin=5V, the transistor will be on because there is sufficient potential available at the base the turn the transistor on. A base current of $\frac{5V - 0.6V}{6.8K\Omega} = 0.647mA$ will flow. If the transistor is saturated, its collector will be at 0.2V, putting 8-.2=7.8V across the 820Ω resistor. This will cause 9.5mA to flow through the 820Ω resistor. Of that, $\frac{0.2V}{1500\Omega} = 0.133mA$ will flow through the 1500Ω resistor, leaving 9.366mA to flow through the collector. This yield a Base:Collector current ratio of 1:14.47, which falls within the acceptable range to call saturation.

b) If Vin =-5V, the transistor will be off because the Base:Emitter junction will be reverse biased. The output voltage will be set by the voltage divider formed by the 820Ω & 1500Ω resistors and accounting for the transistor off state leakage current . $\frac{8V - V_c}{820\Omega} = \frac{V_c}{1500} + 100\mu A \;\; V_c = 5.12V$.

c)When Vin=12V, the ΔV across the input resistor is 12-0.6=11.4V, therefore the current is 1.68mA flowing into the base of the transistor.

d) When the input is at -25V, the base of the transistor will be held to -0.6V by the 1N4001, so the DV across the resistor is 25-0.6=24.4V, therefore the current is 3.59mA flowing towards Vin.

e) The equivalent resistance seen by the output capacitor will be the parallel combination of 820Ω and 1500Ω, or 530Ω. So τ= 530Ω * 20pF = 1.06E^{-8}S. The 10%-90% rise time is 2.2τ or 23.3nS

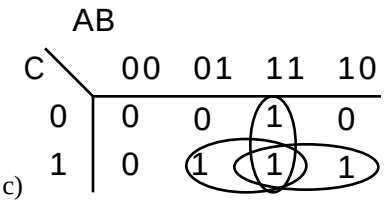
Problem #5

a)

A	B	C	M
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

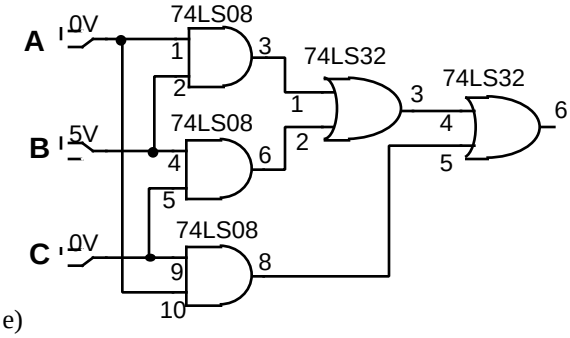
b) $(A \cdot B \cdot C) + (A \cdot B \cdot \overline{C}) + (A \cdot \overline{B} \cdot C) + (\overline{A} \cdot B \cdot C)$

c)



d) $(A \cdot B) + (A \cdot C) + (B \cdot C)$

e)



Problem #6

a) Maximum current will flow when two of the transistors in the bridge are saturated. With V2 at a high enough potential, the upper left & lower right transistors will be on and saturated, providing 5-.2-.2=4.6V across the 27Ω resistor. This will cause 170mA to flow through R_7. Using the 10:1 rule of thumb, this will require 17mA of base current in both the upper left & lower right transistors. 17mA through 220Ω will result in a 3.74V drop across R6. This means that we need 3.74 + 0.6V or 4.34V at V2 to get the lower right transistor into saturation. With this voltage at V2, we will get 4.34V-0.6V = 3.74V across R2, which will result in 1.7mA flowing into its base. This is enough to support the required collector current of 17mA needed to put the upper left transistor into saturation. The current through R3 (the base current for the upper left transistor) will be $\frac{5V - 0.6V - 0.2V}{220\Omega} = 19mA$. This leaves us with a 1:8.9 ratio on the upper transistor, 1:11.2 ratio on the helper transistor and 1:10 on the lower right transistor. All sufficient for saturation.

b)170mA flow left to right

c)Since that transistor is on, the base will be 0.6V below the emitter, which is at 5V, so 5-0.6=4.4V

d)Source 17ma + 1.7ma = 18.7mA

e) 0, there would be no potential across the resistor, but there would be massive current flowing through the bridge transistors.

Problem #7

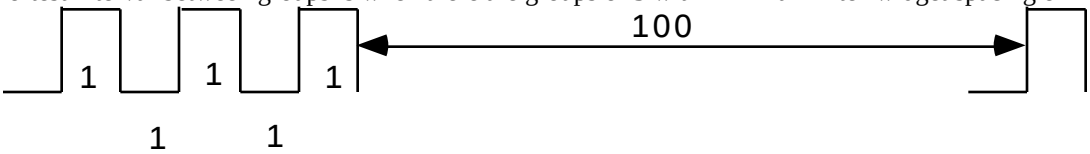
The minimum size for the resistor is set by the current sinking capabilities of the LS05 in the low state. This is 8ma. From this we must subtract the input current that will be coming from the 74C04s (-1μA each) leaving 7.997mA that could be sunk from the pull-up resistor. The voltage across the pull-up resistor will be 5V-0.35V = 4.65V(I have taken the typical value since it is more conservative than the max. value). Therefore R_{min} is $\frac{4.65V}{7.997mA} = 581\Omega$.

The maximum size for the resistor is set by the combination of the input current and voltage requirements of the 74C04s and the leakage current of the '05. They require 1μA per input at 3.5V (with a 5V power supply) and the '05 leaks 100μA. So the maximum resistor size is $\frac{5V - 3.5V}{103\mu A} = 14.56K\Omega$.

The rise time requirement implies a τ of $\frac{50nS}{2.2} = 22.7nS$. The input capacitance of each 74C04 is 6pF for a total of 18pF. Since τ=RC, the largest resistor that will satisfy the rise time requirement is $\frac{\tau}{18pF} = \frac{22.7nS}{18pF} = 1263\Omega$. I would choose 1.2KΩ as the closest standard size. This will be the minimum power dissipation solution because it is the largest value that will meet the rise-time requirements.

Problem #8

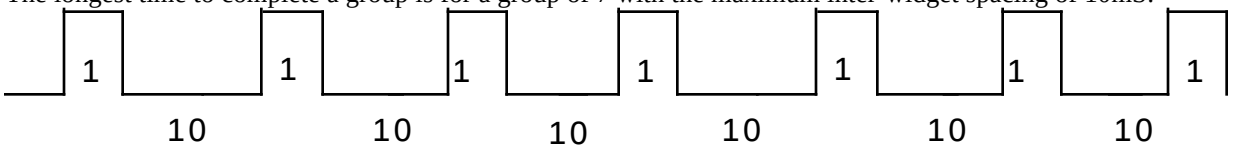
The shortest interval between groups is when there are groups of 3 with minimum inter-widget spacing of



1mS :

which yields a minimum time between first elements of 105mS.

The longest time to complete a group is for a group of 7 with the maximum inter-widget spacing of 10mS:



which yields a maximum time from first element to last element of 67mS.

Therefore between 67mS & 105mS after the first member of a group is a period when we are guaranteed the input will be low. So, set up a 555 One-Shot (Mono-stable) to fire between 67 & 105mS (I chose 86mS). The falling edge of that pulse will trigger a 2nd 555 one-shot to time the output pulse for 1mS. The output of that 555 will gate the recognition logic for 3,5 & 7 elements. Finally, the falling edge of the output of the 2nd 555 will trigger a final 555 to generate another 1mS pulse to reset the '161 counter.