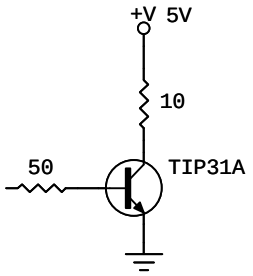
ME218a 1997 Final Exam Solution

Problem 1 (10pts)

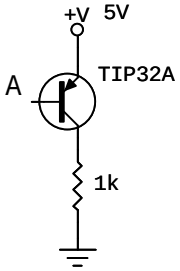


You encounter an output circuit like the one shown above.

a) What measurement(s) of the nodes shown would you make to determine whether or not the transistor is in saturation ?
b) If you could only make a single measurement, what would it be and what value (or range) would you expect if the transistor was in saturation ?

a) measure the collector voltage, look for small V_{ce}; measure the voltage drop across the 10Ω resistor and the 50 Ω resistor, use these to calculate the base:collector current ratio
b) measure the collector voltage, look for small V_{ce} (0.1V for 500mA I_c).

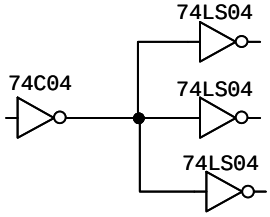
Problem 2 (10pts)



a) What voltage is necessary at point A to force the TIP32 into saturation ?
b) What current (direction and magnitude) must be sourced/sunk at point A to force the TIP32 into saturation ?

a) from Fig. 10 in the TIP32 data sheet, V_{be} at about 5mA I_c will be about 0.53V, so that the voltage at point A will be **4.47V**.
b) from Fig. 10 in the TIP32 data sheet, V_{ce} at about 5mA I_c will be about 0.13V, so that the voltage at the collector lead will be 4.87V, resulting in 4.87mA through the 1k resistor. To maintain a 10:1 collector:base current ratio, **0.487mA** should be **sunk** from the base at point A.

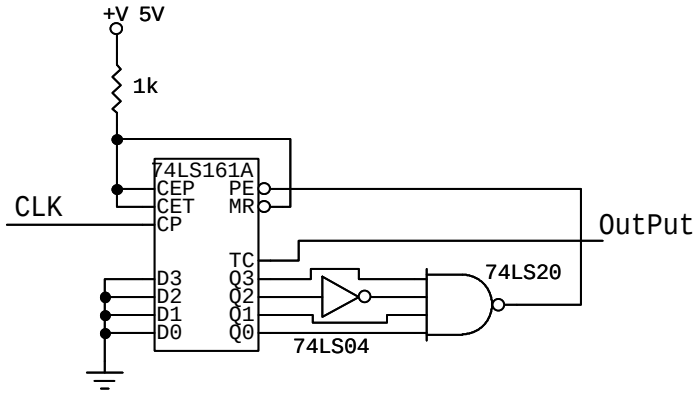
Problem 3 (5pts)



Can you explain to your lab-bench partner why their circuit (above) is not working ? Be very specific about the details, quoting specifiations.

From the data sheet provided w/ Lab 1, the I_{IL} for the 74LS04 is 0.36mA when V_{IL} =0.4V. Three such gates would require the 74C04 output to sink 1.08mA. From the 74C04 data sheet, in the CMOS to Low power section, the output voltage is listed as 0.4Vwith a corresponding output current of 360μA. 1.08mA >> 360 μA, so the 74C04 output is overloaded by this circuit.

Problem 4 (10pts)



What is the maximum clock frequency, without exceeding specifications, for this circuit ?

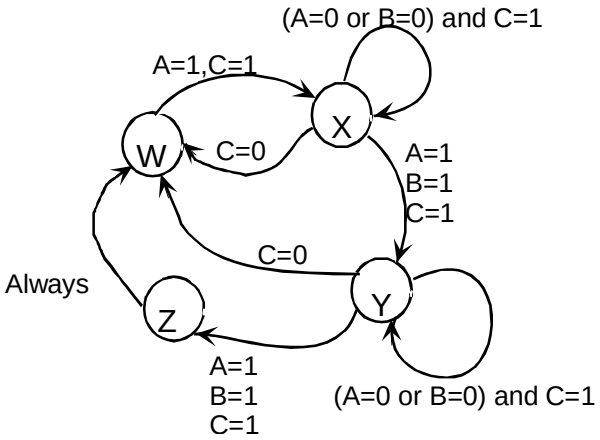
The clock period can not be allowed to exceed the time for the result to propagate through the '161, '04 and '20 and meet the set-up time at PE. Max period = $T_{pd161} + T_{pd04} + T_{pd20} + T_{su161}$ = 27nS + 10nS + 10nS + 25nS = 72nS; **F=13.89MHz**

Problem 5 (5pts)

Describe the output signal from the circuit in problem 4.

The TC pin will go high when the count on the Q outputs is 1111. In the circuit above, when the count is 1011, the PE pin will be asserted and on the next clock pulse, the count will be reset to 0000. Therefore, the count will never be 1111, so **the output will be a constant low.**

Problem 6 (15pts)



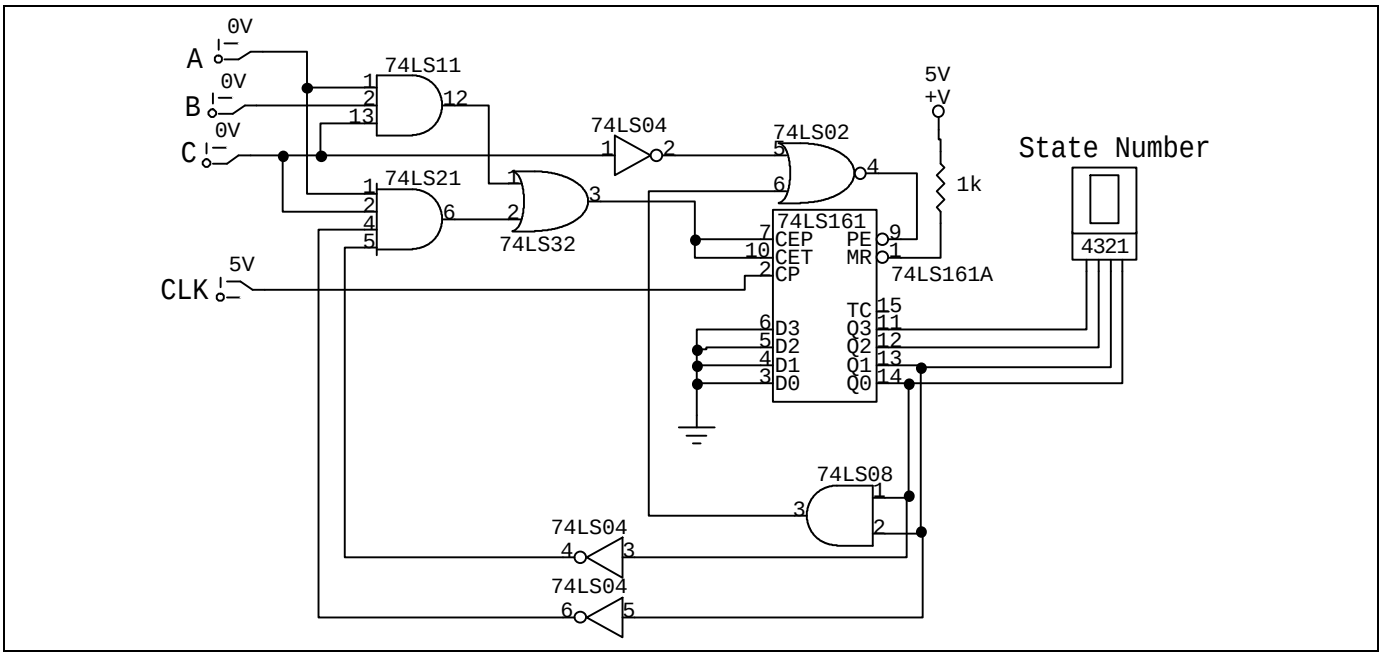
Given the 3 logic inputs, A,B,C and a clock, design a circuit to implement this state machine. Minimize the logic required.

The problem has 4 states requiring 2 bits to track. This easily fits into a '161 counter. The next task is to assign states. Since 3 paths enter state W, it will be simplest to assign state W to 00, that way we can use the PE input to load zeros. By examination, we can see that state W will be entered when C=0 or when the state is 11. We can use this knowledge to construct the control line to the PE input on the '161. Looking at the diagram we can construct a Karnaugh Map that shows what combinations of states and inputs result in transitioning to a new state:

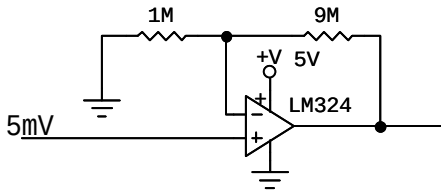
A,B,C->	000	001	011	010	110	111	101	100
00(W)	0	0	0	0	0	1	1	0
01(X)	0	0	0	0	0	1	0	0
11(Z)	1	1	1	1	1	1	1	1
10(Y)	0	0	0	0	0	1	0	0

The Z row is already covered by the transition to state 0, so we are left needing only 2 terms to control CEP & CET:

$A \bullet C \bullet \overline{Q}_0 \bullet \overline{Q}_1$ or $A \bullet B \bullet C$



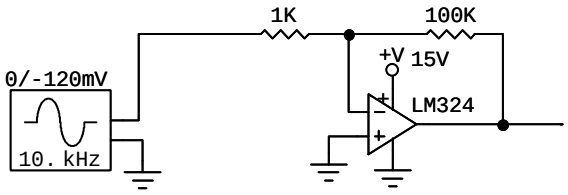
Problem 7 (10pts)



What voltage would you expect at the output of the LM324 ?

The circuit has a gain of 10, so the 5mV input would normally produce an output voltage of 50mV. However, the large size of the feedback resistors will generate an offset between the two inputs to the op-amp. We would expect to see a voltage at the inverting input that would be due to the input bias current flowing through the equivalent resistance of the feedback network. ((1MΩ || 9MΩ = 900kΩ) * 250nA) = 225mV. This puts the non-inverting input 220mV below the inverting input, driving the output toward the lower rail. V_{ol} for the LM324 is a maximum of 20mV, so **the output should be between 0 & 20mV.**

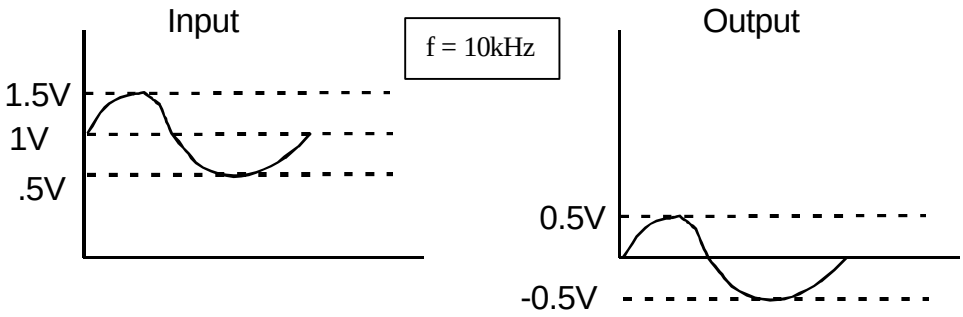
Problem 8 (10pts)



Describe the output amplitude of the LM324 in this circuit.

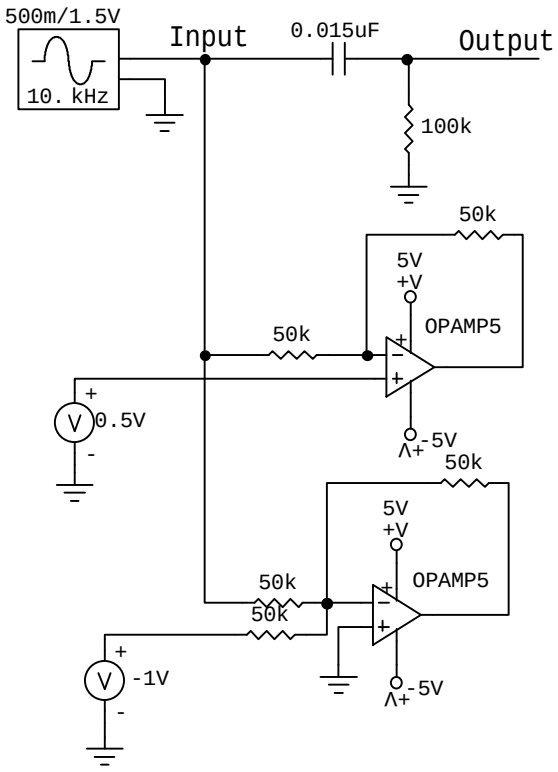
The circuit has a gain of –100, with an input voltage of –120mV, the output would normally be 12V. However, with this large an output voltage swing, the slew rate of the amplifier comes into play. From Figure 3 of the LM324 data sheet we see that at 10kHz, the slew rate limits the output **amplitude to about 9.3V.**

Problem 9 (10pts)



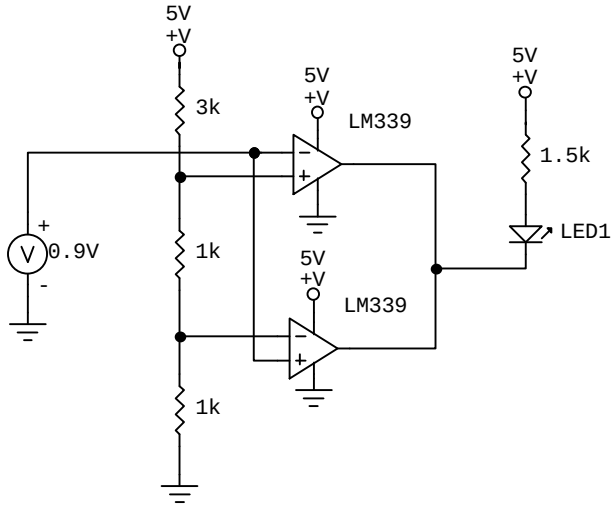
Show 2 different circuit designs (including component values) that would transform the input signal into the output signal with no more than 1% error in amplitude. Phase is unimportant, and you may ignore component tolerances.

The simplest solution is just a high pass filter, with a corner frequency set such that there is 1% or less attenuation at 10kHz:



Sizing the resistor/capacitor pair is a matter of deciding on the desired minimum impedance and setting R to that. Then C can be calculated by noting the voltage divider that is formed and dealing with the impedance of C ($1/j\omega C$).
The second part of the circuit is an inverting amplifier with an offset.
The third part of the circuit is a summing amplifier that sums in –1V to remove the 1V offset of the input.
The last two circuits produce identical output waveforms that are in phase with the input. The Hi-Pass filter produces an output that is phase shifted by 180° from the input waveform.

Problem 10 (15pts)
Design a circuit that will light an LED (V_f = 1.5V @ 2mA) when an input voltage is greater than 2V or less than 1V.



This is simply a window comparator. The lower comparator's output is low (and therefore the LED is lit) if the input voltage is less than 1V. The upper comparator's output will be low if the input voltage is above 2V. Between 1 & 2V, both comparator outputs will be high, and the LED will be off.