## ME218a 1998 Midterm Solution

## Problem \#1 15 Points



The input to your circuit should be a 1 Mhz Square Wave.
The first thing to notice is that the period of the repeating waveform is $12 \mu \mathrm{~S}$. This will require a modulo 12 counter. While there are many ways to achieve this, probably the simplest is to use the synchronous load capabilities of the 161 (or the synchronous reset of the 163). This will require defining logic to recognize the state of 11 , since the counter should count $0-11$, then repeat. Eleven is a state of 1011 on $\mathrm{Q}_{0}-\mathrm{Q}_{3}$. Having done that we need to define logic that will produce a high output corresponding to the desired waveform. Recognizing any of the many combinations of counts that would give the desired relationship could do this. The easiest to use is simply 0,1 and $6,7,8$. To find the simplest logic to recognize these, make a Karnaugh map.


From this, we can read off the expressions for the output: $\overline{(Q 0} * \overline{Q 1} * \overline{Q 2})+(\overline{Q 3} * \overline{Q 2} * \overline{Q 1})+(\overline{Q 3} * Q 2 * Q 1)$. We can implement this in the obvious way, as shown below.


However, this solution has a subtle problem (one I did not catch myself until I looked closely (I don't expect you to have caught it)). As the count moves from 7 to 8 , the true output moves between the min-terms $\mathrm{A}(\overline{Q 3} * Q 2 * Q 1)$ and $\mathrm{B}(\overline{Q 3} * \overline{Q 2} * \overline{Q 1})$.

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The subtlety has to do with the fact that the first min-term has True versions of Q2 \& Q1, while the second minterm has inverted versions of all of its inputs. 1 'LS11 propagation delay after the count changes the minterm from gate A will go false. The minterm from gate B will not go true until 1 'LS04 propagation delay later. As a result, the output will have a glitch in it every time the count transitions from 7 to 8 . The problem is that we are moving between minterms with different propagation delays. We could fix the problem by modifying one of the minterms so that its propagation delay matched that of the other. Here is a good place to apply DeMorgans Theorem. We can take $(\overline{Q 3} * \overline{Q 2} * \overline{Q 1})$ and transform it into $(\overline{Q 3+Q 2+Q 1})$. This is a NOR gate with True inputs so now as the A gate output disappears, the B gate output will appear, and we eliminate the glitch.


## Comments on your solutions:

Many people tried to make this much more complicated than it needed to be. I had thought that this was a straight-forward extension of the waveform generation problem that we worked in class. All that was needed was to recognize two sets of states to generate the output, rather than the one of the example.

The most common problems were:

1) not using the synchronous pre-load
2) Karnaugh map problems with not recognizing wrap-around pairs. This didn't cause wrong answers, just expressions that could have been simplified further.

Other than that, most of the real problems arose in the course of executing those one-of-a-kind solutions, and as such were not "common" to any other person's solution.

The mean score on this problem was 12.2 out of 15 , with $38 \%$ of the class getting full credit for the problem

## Problem \#2 10 Points

Given the output of a 74 C 04 as a control, design the necessary circuitry to power a load with a resistance of $14.5 \Omega$ and requiring at least 1 A to actuate when the output of the 74 C 04 is high. You have a 15 V supply available.
The 74C04 has so little current drive capability, especially in the high state, that we are going to need a LOT of current gain $\left(\frac{1 A}{360 \mu}=2,778\right.$, requiring multiple bi-polar transistors) or, we could use a voltage controlled device (i.e. MOSFET). This is clearly the better solution.


With its very low ON resistance, the MOSFET will represent less than 50 mV drop at 1 A , making most of the 15 V available for the load. This will be more than enough to meet the minimum 1A current through the load.

## Comments on your solutions:

Far and away the most common mistake was to use the short circuit output current ( 1.75 mA ) for the ' C 04 . In this context, this is a useless spec. If we are trying to use a bi-polar transistor, we need both a certain amount of voltage as well as current. The output short circuit curent is spec'd. with the output at 0 Volts.

The mean score on this problem was 6.3 out of $10,39 \%$ of the class got full credit for this problem.

## Problem \#3 15 Points

You have been asked to size the pull-down resistor that will be placed on the input of a 74HC14. The pull-down resistor should guarantee a logic low input to the 74 HC 14 when there is nothing else connected to the 'HC14 input. From time to time, there will an 'HC14 output connected to this input, under those conditions, your pull-down resistor should not add more than $50 \mu \mathrm{~A}$ to the input current required by the ' HC 14 .

The situation described can be modeled as


Our task is to size R1. When the switch is open R1 must be small enough to allow the input current from the right hand 74 HC 14 to pass to ground without creating so much drop that it won't be interpreted as a low. For the 74 HC 14 , that means that we are interested in the minimum negative going threshold. The voltage drop must be less than $\mathrm{V}_{\mathrm{T} \text {-. so }}$
$R_{\max }=\frac{V_{T-}}{I_{i n}}=\frac{0.9 \mathrm{~V}}{1 \mu A}=900 \mathrm{k} \Omega$ (I used the maximum input current over temperature). When the switch is closed, the resistor
should not add more than $50 \mu \mathrm{~A}$ to the amount that the right hand 'HC14 has to provide. For this we need to know what the output voltage will be from the ' HC 14 when it is driving $50 \mu \mathrm{~A}+$ the $\operatorname{Iih}(1 \mu \mathrm{~A})$ of the 74 HC 14 . The data sheet provides two sets of output voltage spec's., one at $-20 \mu \mathrm{~A}$ ouput current and one at -4 mA output current. If we are going to limit the load to $51 \mu \mathrm{~A}$, we can't use the spec's at $-20 \mu \mathrm{~A}$, so we choose the voltage spec. at 4 mA . The minimum value for the resistor will then be $R_{\min }=\frac{V_{o h}}{50 \mu A}=\frac{3.84 V}{50 \mu A}=76800 \Omega$. Technically, any value in between these extremes will satisfy the requirements.
However, the maximum value is outside our guidelines values for typical resistor values (a few hundred $\Omega$ to a few hundred $\mathrm{k} \Omega$ ) so I would choose the next largest standard value above the minimum, $82 \mathrm{k} \Omega$.

## Comments on your solutions:

Many people used 5 V rather than $\mathrm{V}_{\text {oh }}$ for the driving device. Some of you quoted a $\mathrm{V}_{\mathrm{il}}$ spec. rather than $\mathrm{V}_{\mathrm{t}}$ which leads me to believe that you were not reading the 74 HC 14 data sheet.

The mean score on this problem was 7.6 out of $10,30 \%$ of the class got full credit for this problem.

## Problem \#4 15 Points

You have a signal of interest that is a sine wave at 16 kHz of 1 V ( $\mathrm{pk}-\mathrm{pk)}$ amplitude, centered at 0 V . However, it is corrupted by 50 Hz noise (superimposed) with an amplitude of 100 mV .
Design the simplest possible filter that will reduce the noise level to no more than 5 mV , while introducing no more than $3 \%$ loss in the 16 kHz signal. The output should also be shifted to be centered around 2.5 V .

The first thing to recognize here is that what we need is a high pass filter that will pass the 16 kHz , while attenuating the 50 Hz noise. There are at least three possible approaches to designing the filter:

1) Start with the desired attenuation of the 50 Hz and then check for the signal loss
2) Start with the loss limit and then check the noise signal for meeting the attenuation spec.
3) Calculate the Min \& Max RC products to meet the signal loss \& attenuation specs., check to be sure that there is a range between.
I chose approach \#3 which encompasses \#1 \& \#2.
We can use the standard expression relating $\mathrm{V}_{\text {in }}$ to $\mathrm{V}_{\text {out }}$ for a high-pass filter to calculate the required time constant for the
filter. $V_{\text {out }}=\frac{2 \pi f R C}{1} V_{\text {in }}$

$$
\left[1+(2 \pi f R C)^{2}\right]^{\frac{1}{2}}
$$

at $50 \mathrm{~Hz}, \mathrm{~V}_{\text {in }}=100 \mathrm{mV}$ \& $\mathrm{V}_{\text {out }}$ must be $<=5 \mathrm{mV}$; at $16 \mathrm{kHz}, \mathrm{V}_{\text {in }}=1 \mathrm{~V} \& \mathrm{~V}_{\text {out }}$ must be $>=0.97 \mathrm{~V}$
For this to be useful, you need to rearrange to be able to solve for RC. Start by expressing things in terms of Vout/Vin:
$\frac{V_{\text {out }}}{V_{\text {in }}}=\frac{2 \pi f R C}{\left[1+(2 \pi f R C)^{2}\right]^{\frac{1}{2}}}$
to simplify the algebra, substitute X for the Vout/Vin ratio, A for $2 \pi f$, B for RC , then get rid of the square root in the denominator:

$$
X^{2}=\frac{(A B)^{2}}{1+(A B)^{2}}
$$

re-arranging to isolate B :

$$
B^{2}=\frac{X^{2}}{A^{2}\left(1-X^{2}\right)}
$$

re-placing the original components:
$R C^{2}=\frac{\left(\frac{V_{\text {out }}}{V_{\text {in }}}\right)^{2}}{(2 \pi f)^{2}\left(1-\left(\frac{V_{\text {out }}}{V_{\text {in }}}\right)^{2}\right)}$
$R C=\sqrt{\frac{\left(\frac{V_{\text {out }}}{V_{\text {in }}}\right)^{2}}{(2 \pi f)^{2}\left(1-\left(\frac{V_{\text {out }}}{V_{\text {in }}}\right)^{2}\right)}}$
Now we have an expression into which we can plug the desired performance and determine the required RC.
At 50 Hz we can calculate the maximum RC that will give us the required attenuation:
$R C=\sqrt{\frac{\left(\frac{5 m V}{100 m V}\right)^{2}}{(2 \pi 50 \mathrm{~Hz})^{2}\left(1-\left(\frac{5 m V}{100 m V}\right)^{2}\right)}}=1.6 \times 10^{-4} S$

At 16 kHz we can calculate the minimum RC that will give us no more the $3 \%$ loss:
$R C=\sqrt{\frac{\left(\frac{0.97 V}{1 V}\right)^{2}}{(2 \pi 16 \mathrm{kHz})^{2}\left(1-\left(\frac{0.97 V}{1 V}\right)^{2}\right)}}=4.0 \times 10^{-5} S$

Any RC that falls between these values will meet the frequency response specifications.

The offset from a 0 reference to a 2.5 V reference is easily accomplished using a configuration that you saw in the Lab 0 as well as in lecture:


In order to use standard values, I chose to use an RC of $1.5 x 10^{-4} S$. Note: the R in this is expression is the $\mathrm{R}_{\mathrm{eq}}$ of the voltage divider resistors that give the DC offset.

## Comments on your solutions:

Many of you tacked on voltage dividers to your high pass filters, without considering the effects on the corner frequency. Another common failure mode was to start with the complex impedances (not necessarily bad), but then got lost in the math.

Many of you tried things with diodes, like these:

this gives an output centered about 5 V

output centered about $1.5 \mathrm{~V} \&$ introduces non-linearitites.
The mean score on this problem was 10.5 out of $15,35 \%$ of the class got full credit for this problem.

## Problem \#5 10 Points

Given an LTR-3208E photo transistor, design a circuit the will provide a clean logic level 0 to logic level 1 transition as the light level changes from 0 to $1 \mathrm{~mW} / \mathrm{cm}^{2}$ respectively. Show calculations and call out relevant specifications.

Here we need to use the phototransistor to change the input voltage to a Schmitt trigger input. We need a Schmitt trigger, because of the spec for a clean logic level transition and the slow speed of rise \& fall of the phototransistor. Since the simplest Schmitt trigger device is an inverter, we need to pull the input low with increasing light in order to make the output go high.


What remains is to size the pull-up resistor. The minimum value for the pull-up is determined by the maximum current that we can expect the phototransistor to sink. From the data sheet we can see that the phototransistor will be saturated at $0.5 \mathrm{~mA} \mathrm{I}_{\mathrm{ce}}$ with $0.5 \mathrm{~mW} / \mathrm{cm}^{2}$ illumination. Under these conditions, the $\mathrm{V}_{\mathrm{ce}}$ will be 0.4 V , a legal low for all logic device that we have studied. Since we have more than $0.5 \mathrm{~mW} / \mathrm{cm} 2$ illumination, if we limit the current through the phototransistor to 0.5 mA , it should be saturated. That 0.5 mA will be coming from the input low $\mathrm{I}_{\mathrm{il}}$ of the Schmitt trigger and the pull-up resistor. Using the data from a 74 HC 14 (others may work as well) we see that the worst case input low current is $1 \mu \mathrm{~A}$, leaving essentially the entire 0.5 mA to come from the resistor. The resistor may be as small as $\frac{5-0.4}{.5 m A-1 \mu A}=9200 \Omega$. In the light off state, the pull-up will need to supply both the input high current, $\mathrm{I}_{\mathrm{i} h}$, to the Schmitt trigger as well as the dark leakage current through the phototransistor. Under these conditions, the voltage drop across the pull-up must be low enough to guarantee a legal high to the Schmitt trigger. The worst case input high voltage required by the 74 HC 14 is 3.15 V , so with $5-3.15=1.85 \mathrm{~V}$ across the resistor Iih $(1 . \mu \mathrm{A})+\mathrm{I}_{\text {CEO }}$ $(0.1 \mu \mathrm{~A})$ should flow. The maximum value for the resistor is $\frac{5-3.15}{1 \mu A+0.1 \mu A}=1681818 \Omega$. This is larger than the values that we would like to be working with, so I would once again choose the next larger standard size above the minimum ( $1 \mathrm{k} \Omega$ ), though any value between the two calculated extremes will work.

## Comments on your solutions:

Some people used 1 mA as the saturated current instead of 0.5 mA , they were probably looking at the spec for current as a function of light, failing to notice that those specs apply at a Vce of 5 V .
-Other folks failed to calculate the bounds of the pull-up resistor (instead, lots of people picked a resistor and then showed that it worked on one of the two bounds)
Forgetting leakage currents or not using the correct leakage currents.
Not using a Schmitt trigger input device for the clean edge.
The mean score on this problem was5 out of 10 , only 3 people got full credit for this problem.

## Problem \#6 10 Points

$\square$
Design a circuit that will produce a 0.5 S high pulse for every input pulse like that shown below:


These pluses will occur at random intervals, but never separated by less than 0.5 S .
This is the perfect place for the mono-stable configuration of a 555 . The delay is calculated as 1.1 RC ,so $\mathrm{RC}=0.45$, if $\mathrm{C}=2.2 \mu \mathrm{~F}$, then $\mathrm{R}=204545 \Omega$, choosing the closest standard value of $200 \mathrm{k} \Omega$, yields a pulse width of $1.1(200 \mathrm{k} \Omega * 2.2 \mu \mathrm{~F})=0.484 \mathrm{~S}$. I chose to go down to 200 k rather than up to 210 k because, for proper operation, the next trigger to the 555 should not come before the prior pulse has completed. With a $210 \mathrm{k} \Omega$ resistor, the pulse would have been slightly longer than 0.5 S .


## Comments on your solutions:

Some people calculated the delay as RC instead of 1.1 RC .
Some people tried to do it with counters and magical-mystical square waves out of thin air.
The mean score on this problem was 9 out of $10,73 \%$ of the class got full credit for this problem.

## Problem \#7 25 Points

You have been asked to design the logic for a speed regulator. The input to your circuit will be a pulse train coming from the motor that is being controlled. The goal is to control the speed of the motor such that the pulse train is at approximately 100 Hz . At a constant speed, this signal will be a square wave. Your regulator circuit should produce two outputs: Accelerate and Brake. If the speed is less than 96 Hz , you should activate (set high) the Accelerate line and not the Brake Line. If the speed is at or above 120 Hz , you should activate (set high) the Brake line and not the Accelerate Line. If the speed is within the range, neither signal should be active. Based on the inertia of the driven system, you have been told that the command signals must be updated at least 8 times a second and that the maximum acceleration/deceleration rate is $40 \mathrm{~Hz} / \mathrm{Sec}$.. From another part of the system, a highly accurate 32.768 kHz square wave is available for your use. Complete your design using HC family logic devices. Be sure to label all IC pins in your schematic with their functional label, not just pin numbers.
Note: Don't get carried away with misplaced accuracy here. Take a look at the width of the acceptable speed range. Consider the impact of the conditions that you are evaluating. For instance, if you are at 96 Hz and you fail to remove the accelerate signal: no big deal, you will continue to accelerate for another $1 / 8 \mathrm{sec}$. taking you to 101 Hz , where you should certainly remove the accelerate signal. Remember: start with blocks identifying the functions that you need.

The spec. says that we need to evaluate the speed every $1 / 8 \mathrm{sec}$., so we'll need a block to trigger the evaluation. We'll also need a counter to count the speed pulses during the $1 / 8^{\text {th }} \mathrm{S}$ intervals. Then we'll need some logic to decide to accelerate, brake or do nothing, a latch to capture $\&$ hold the brake $\&$ accelerate signals until the next evaluation and finally, a way to reset the counter to start counting again for the next $1 / 8^{\text {th }} \mathrm{S}$.


The over-speed logic logic is easy, since it the count of 15 , and TC goes high on a count of 15
The under-speed logic is any count less than 12. Using a Karnaugh map, I reduced this to $\overline{Q_{3}} \oplus\left(Q_{3} \bullet \overline{Q_{2}}\right)$


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The 74 HC 404 divides down the 32.768 kHz signal to get us an 8 Hz signal. The ' $\mathrm{HC} 74+$ ' HC 08 next to it act as a rising edge detector (just like we did in class). In this case, we can predict the width of the pulse, it will be the clock period minus the propagation delay through the '4040. This signal is used to latch the evaluation logic \& an inverted version resets the 'HC161. Between resets, the ' HC 161 counts motor pulses. The lower bits of logic detect the <12 condition needed to activate Accelerate. The TC connection to PE, with the Ds tied high acts as an over-speed latch. If the count ever gets to 15 (over-speed) it asserts the PE, which on the next clock loads 15 , keeping TC set. MR overrides all other inputs, so TC gets held 'till the next reset pulse. The remaining 'HC74s latch the Brake and Accelerate signals to hold them between reset pulses.

## Comments on your solutions:

Many of you made this problem, as with problem \#1, much more difficult than it needed to be. The most successful at this decided to update at the motor pulse rate, rather than $1 / 8^{\text {th }}$ sec. and set about counting the 32 kHz pulses while the motor was high, or between rising edges of the motor signal. This can work, but it is more complex because you need eight bits of counter to count that number of pulses. More complexity = more chances for error
As an alternative to the ' 4040 , many of you strung together 3 ' 161 s, that worked just fine for generating the 8 Hz update clock. Many of you included logic to catch the counter roll-over that resulted from as over-speed condition. I gave 2 bonus points for getting this right, no points taken off if it was omitted or didn't work.
I ignored the fact that a large number of you failed to show pin numbers on your schematics. As a building or debugging tool, schematics without pin numbers are useless.

## Common Mistakes

Forgetting to reset the '161
Not latching the outputs
Getting the counts wrong
Trying to use the sync load to do reset. If you do this, you can't use a short reset pulse, since you can't guarantee overlap between the reset pulse $\&$ the motor signal. This would be especially true at low motor speeds.
Putting a square wave into the ' 161 reset only allows it to count $1 / 2$ the time.
2 outputs tied together.
Not using HC logic as specified.
Not evaluating every $1 / 8^{\text {th }} \sec$ as specified

The mean score on this problem was 17.7 out of $25,17 \%$ of the class got full credit for this problem.

