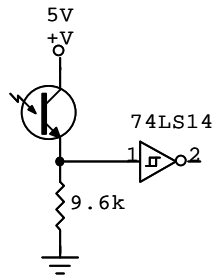
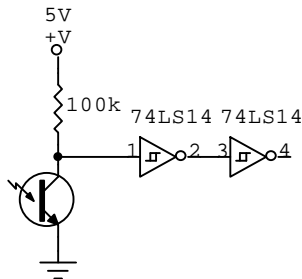


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Problem #1



- From the data sheet, we can see the saturation voltage (V_{ce}) spec of 0.4V, under the conditions of 0.5mA of collector current, with $0.5\text{mW}/\text{cm}^2$ illumination. From the meaning of a saturation spec, we know that adding light beyond the $0.5\text{mW}/\text{cm}^2$ level will not result in a significant drop in the V_{ce} . Therefore, we start by assuming that the V_{ce} will be 0.4V, leaving 4.6V across the 9.6k resistor. This would cause $\frac{4.6\text{V}}{9.6\text{k}} = 0.479\text{mA}$ to flow through the resistor. There would also be up to $20\mu\text{A}$ flowing into the input of the 74LS14, for a total of 0.499mA or approximately the 0.5mA from the saturation spec. From this we can conclude that the transistor is indeed in saturation. With 4.6V at the input, the output of the 74LS14 will be low.
- As we determined in part 1a, the input voltage is 4.6V.
- In this case, the only current through the resistor comes from the input low leakage current from the 74LS14. For the 'LS14, $I_{il} = -0.4\text{mA}$. $0.4\text{mA} * 9.6\text{k} = 3.84\text{V}$.
- The output is still low, because 3.84V is still above V_{th+} for the 74LS14.
- One alternative is to re-arrange the components to make better use of the limited current that the photo-transistor will pass:



When the transistor is illuminated, it will need to pass the I_{il} from the 74LS14 plus the current from the pullup resistor. If it really is saturated, the voltage across it would be 0.4V, so the pullup current would be $\frac{5\text{V} - 0.4\text{V}}{100\text{k}\Omega} = 46\text{mA}$. That, plus

the input low leakage current of 0.4mA is still less than the 0.5mA spec for the transistor in saturation. In the high state the pull-up would hold the 74LS14 input at 2V, while sourcing the required $20\mu\text{A}$ of input current plus the 100nA dark current.

The maximum resistor value would be: $\frac{5\text{V} - 2\text{V}}{20.1\text{mA}} = 149\text{k}\Omega$.

Probably the easiest way to fix this is to find an alternative to the 74LS14. For a 74LS14, the minimum resistor size that would give a legal high is $\frac{2.0\text{V}}{0.5\text{mA}} = 4\text{k}\Omega$. This would result in a no-light voltage of $4\text{k} * 0.4\text{mA} = 1.6\text{V}$, which is too high to be a legal low. Switching to a 74HC14, with its $1\mu\text{A}$ input current solves the problem completely.

Notes on Common Problems:

I think that people got thrown by the phototransistor in this problem. It was not really a phototransistor problem. In fact you needed only 1 spec. from the phototransistor data sheet. The big problem with this problem was the relatively large input current required by the 74LS14.

The places that people lost points most often were:

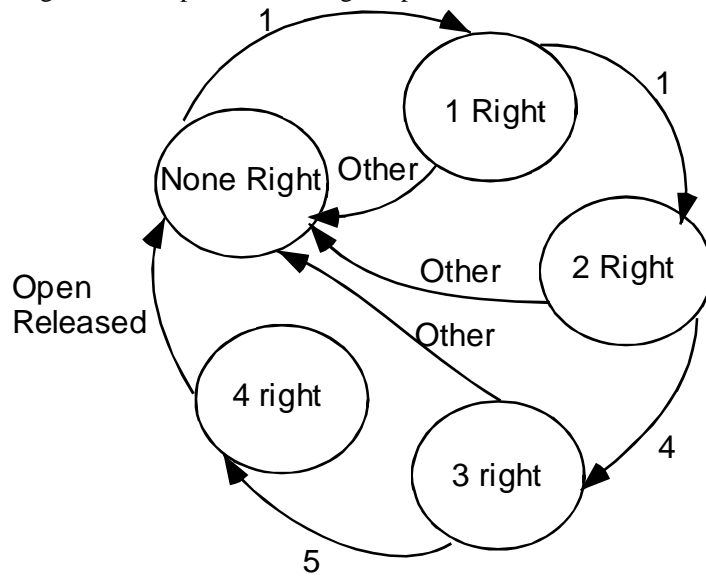
- failing to check for saturation of the phototransistor (yes, it was saturated as originally stated).
- Trying to force 1mA of current through the phototransistor. Many people took the 1mA min. spec for I_c and tried to say that that at least much current was flowing. **It is a Valve Not a Pump !**
- Failing to consider the 74LS14 input low current. This was far and away the most common and significant problem.

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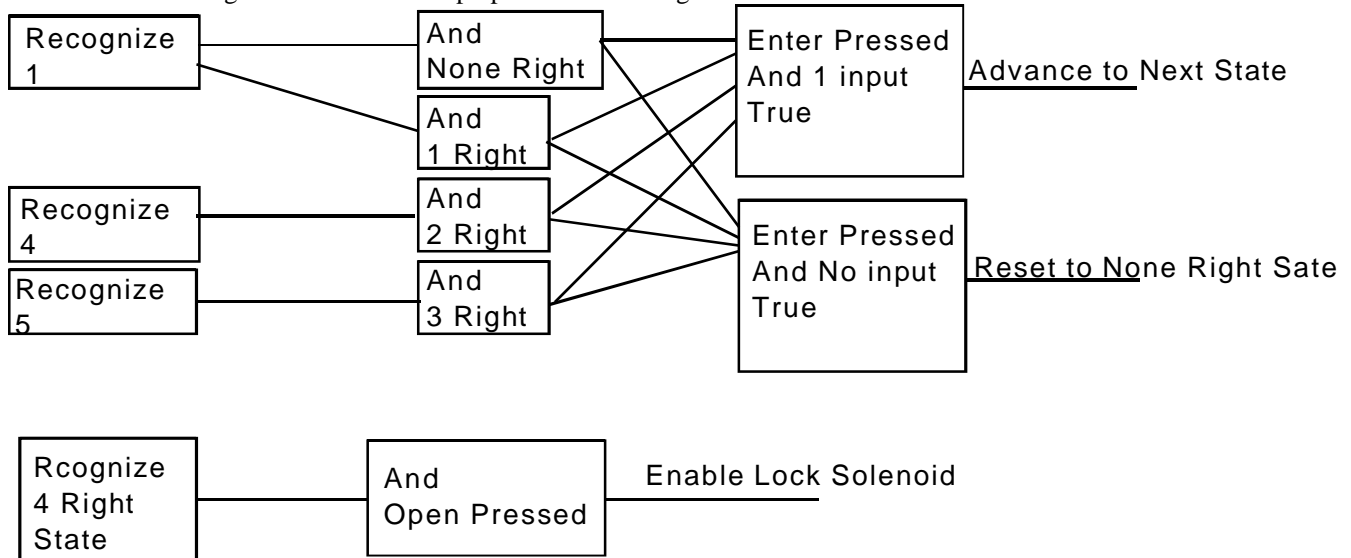
This problem was not a made up example. I saw many people try to build this circuit in their projects last year. It didn't work and I hoped by putting it on the exam to prevent you from making that same mistake.

Problem #2

The problem here is to recognize the state on a set of switches as well as the position within a sequence of the combination. Here is a place where a state diagram can help understanding the problem:

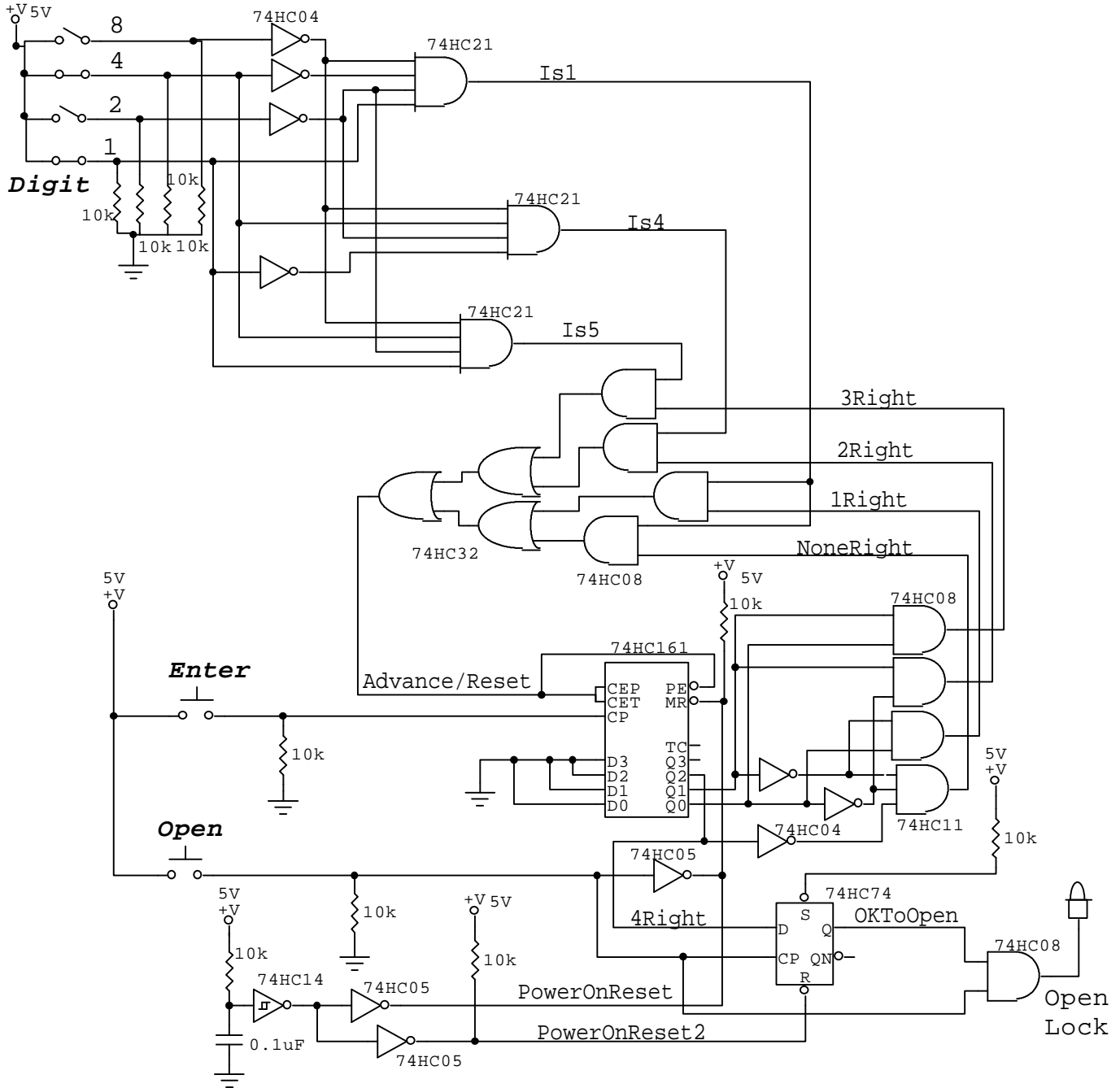


From this we can see that we will need enough flip-flops or counter bits to cover 5 states (3 bits). We can also see that we only want to advance between states if a single condition is met at each state. If that condition is not met, the transition is back to the None Right state. From this I prepared a block diagram like:



Using this guide, I designed the circuit on the following page. Is1, Is4 and Is5 are the logical indicators that one of the valid numbers appears on the switches. Note that the recognition of the valid numbers can not make use of minimization and elimination of the 4th input bit, otherwise it would accept 2 sets of numbers as valid. The 74HC161 counter is used to maintain the state information. Logic on the Q outputs is used to determine which state is currently active. The state information is combined with the switch recognition to determine whether a press of the Enter button will advance to the next state or reset to the None Right state. The fourth bit is used as an indicator that all 4 numbers have been entered. Note that when that bit is set, none of the other states will be recognized, so a press of Enter will reset to None Right. When the Open key is pressed it clocks the state of the 4Right line into the 74HC74 to generate OKToOpen. The 4Right signal is latched because in addition to clocking the 74HC74, the Open key also resets the 74HC161. The OKToOpen signal is combined with the actual state of the Open key to generate the signal to the solenoid. A power-on reset circuit insures that everything starts in a known state. Note that the reset circuit had to be split into 2 parts to prevent the reset of the '161 from resetting the '74

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Notes on Common Problems:

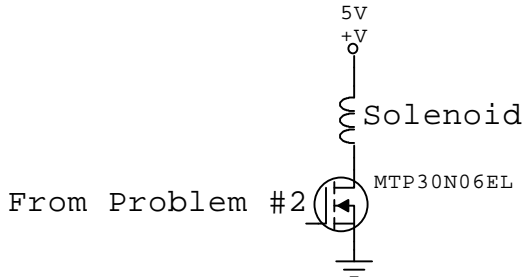
The problem that I think was most common here, was a failure to start with a block-level description of how the circuit should work. This was something that I emphasized in the review session but that I saw relatively few examples of on the exam. Hopefully it was because you simply didn't include that with your solutions. Starting with the conceptual, and documenting it, is an immensely useful tool in solving a problem like this. It allows you to decompose the solution into blocks that are easily understood.

Common Problems:

- 1) building counters out of flip-flops rather than using a counter chip increases the complexity of the circuit, especially if you need features like a synchronous reset or load.
- 2) Not latching the output when the open button is pressed or not triggering the reset on the release of the open button results in a short pulse on the output, rather than an output that is active for as long as the button is down.
- 3) Hooking multiple non-open collector outputs together. Hopefully this is just an oversight in the rush of things.
- 4) Unnecessarily limiting the solution to 2-input gates.

Problem #3

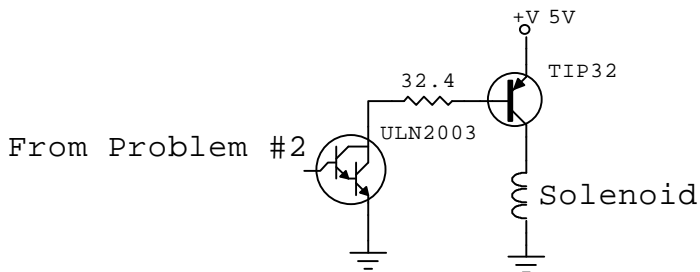
A 1A current through a 4.9Ω consumes 4.9V of the available 5V, leaving a maximum loss across the switching element of 0.1V. This is below the V_{ce} for any of the bi-polar transistors that we have encountered (at least at 1A collector currents). Therefore we need another alternative. Here is the kind of place that a MOSFET shines. If the solenoid current is switched using an MTP30N06VL (data sheet in the lecture notes), then the loss in the switch would be only related to the $R_{ds(on)}$ of the MOSFET, 0.05Ω . At 1A of current, that is a loss of only 0.05V, half of the maximum available. This results in a simple solution:

**Notes on Common Problems:**

This problem, and problem #4 were constructed to bring out the differences between bi-polar and MOSFET transistors. Because of the low voltage available, this problem could only be solved using a MOSFET, with its low on resistance and corresponding low voltage drop. Because we introduced the logic level MOSFETs, there is nothing special that needs to be done to drive the MOSFET, just hook it to the last gate in problem #2. The most common problem that we saw was people trying to use a bi-polar transistor, often in a sourcing configuration. The only power bi-polar transistor that we have introduced had a V_{ce} of 0.2V when conducting 1A, and this is too much drop to be used with a 5V supply to achieve 1A through a 4.9 Ohm load.

Problem #4

In this case, because of the reduced resistance of the solenoid coil, we *do* have sufficient voltage drop available to use a bipolar transistor. However, the requirement that one end of the coil be tied to ground demands that a sourcing configuration be used. A PNP transistor is appropriate in this case. The only PNP transistor capable of 1A available in your lab kit is the TIP32A. However, it is a simple power transistor which will require 100mA of base current to be saturated with 1A of collector current. This is too much current to be sunk by the HC output from problem #2. We will need an additional stage of current amplification. A ULN2003 would be appropriate in this situation. It has a current gain of at least 100, requiring only 1mA to be sourced by the 74 HC08 output from problem #2. This is well within the drive capabilities of the 74HC08. The final circuit is shown below:



The 32.4Ω resistor was sized to limit the base current to 100mA and is based on typical $V_{ce(sat)}$ of 0.9V for the ULN2003 and a typical $V_{be(sat)}$ of 0.86V at 1A collector current and 10:1 Base:Collector current.

Notes on Common Problems:

- 1) trying to use an N-channel MOSFET to source current. This requires a higher than supply voltage to get the MOSFET fully on.
 - 2) Using a TIP32 to drive the load, but failing to notice that it would require 100mA of base current to drive it into saturation. This is too much for a gate to drive, you need another stage of power boost. This is most easily provided by a ULN2003.
 - 3) Failing to account for the real V_{ce} on the ULN2003, just using rule-of-thumb values.
- Many people tried to use the LS05 to directly drive the TIP32, apparently looking at the short circuit current spec. on the '05. This is a bad idea, because the output voltage is not specified or controlled.

