

ME218a Midterm Exam
Due by 5pm on 10/28/94

Name: _____

**I Certify that I have taken this examination in compliance
with the Stanford University Honor Code.**

#1 _____

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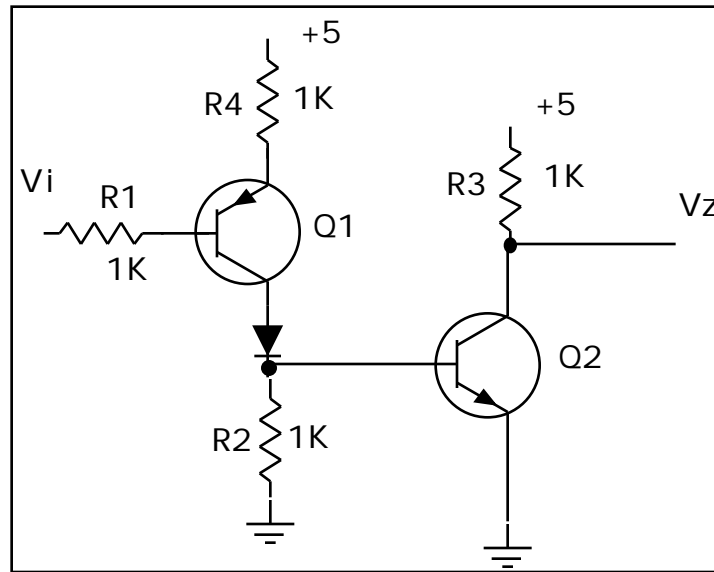
#11 _____

Total _____

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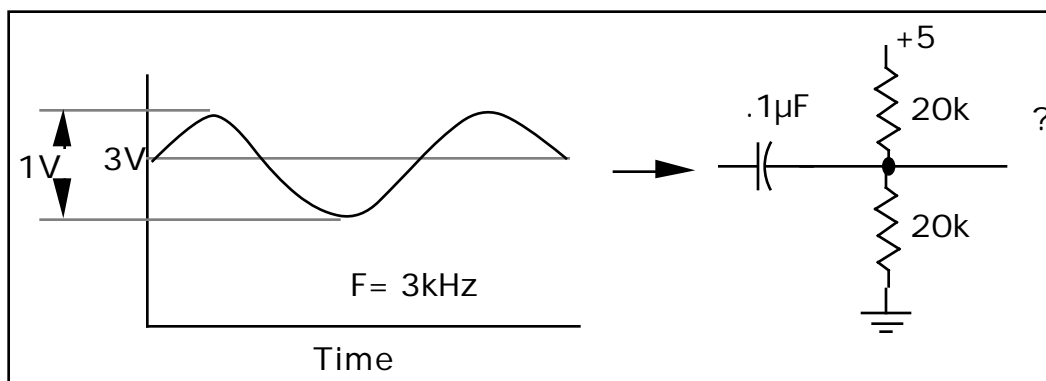
Problem #1 10 Points



In the Circuit above, if $V_i = 0.4V$,

- What is V_z ?
- What is the current in R_2 ?
- Is Q_2 Saturated ?
- What is the current in R_1 ?

Problem #2 5 Points

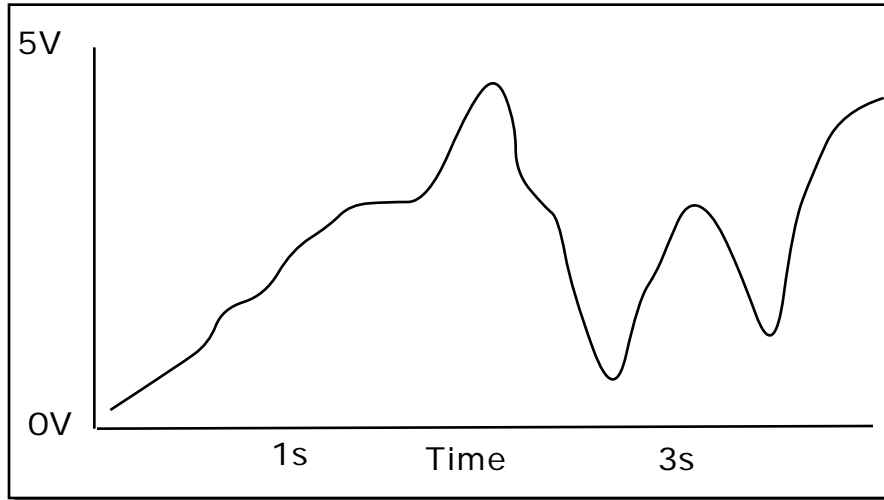


- What is the time constant of this circuit ?
- What is the amplitude of the output ?
- What is the average value of the output ?

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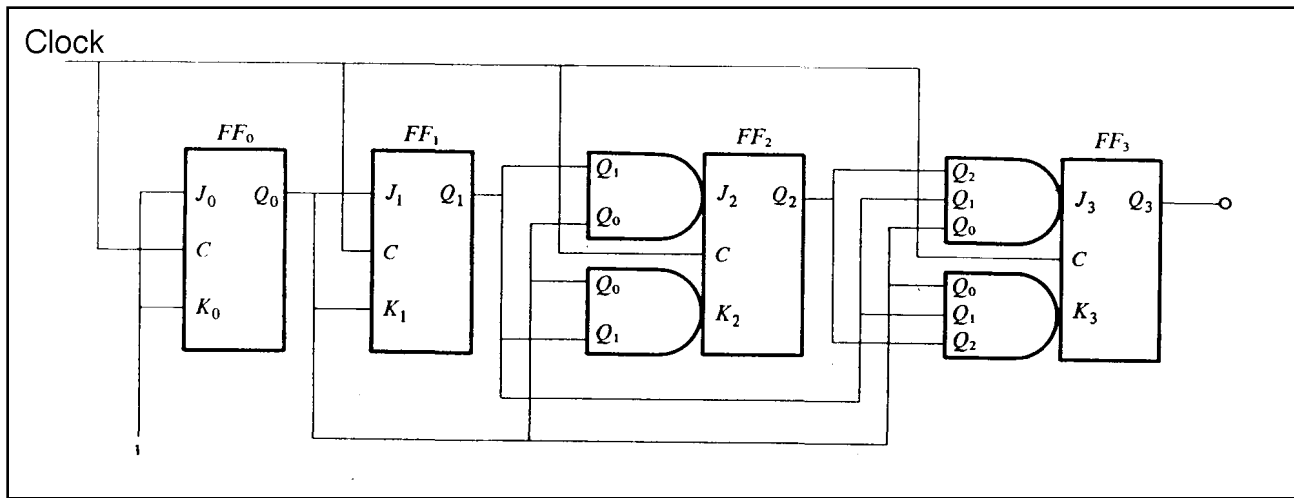
Problem #3 5 Points



Assume the signal above is the input to a 74LS14. Overlay the output behavior. Justify your drawing.

Problem #4 10 Points

For the circuit shown below, assume T_{pd} for the flip flops is 24nS, T_{pd} for the gates is 4nS, T_{su} for the flip flops is 10nS and $T_{pwh} = T_{pwl} = 20nS$ for the flip flops.



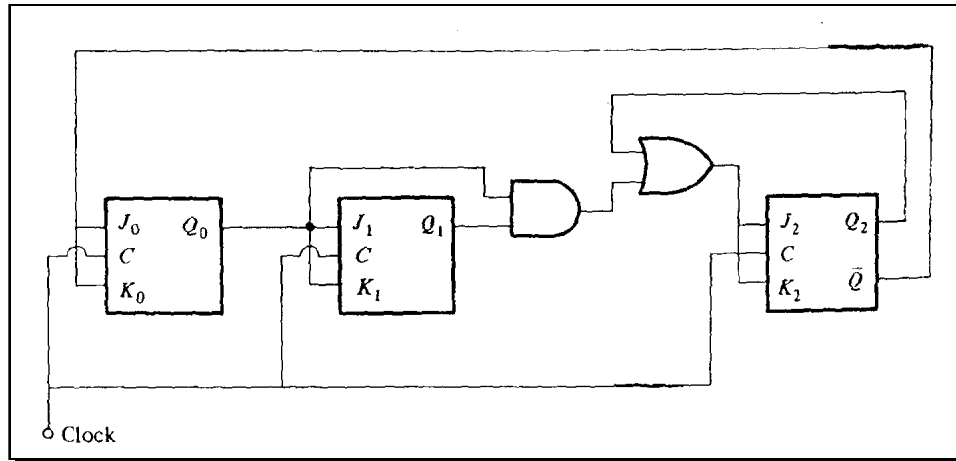
- What is the maximum clock rate for proper operation ?
- Describe, as accurately as possible, the relationship between the rising edges of the clock and Q_0 - Q_3 at any point in time.

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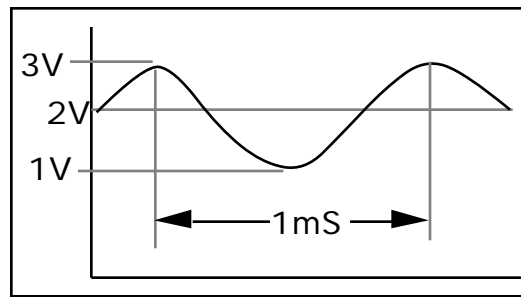
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Problem #5 5 Points

Describe the relations between the clock and Q2 in the circuit below. Use both a state table and a concise textual description.



Problem #6 5 Points

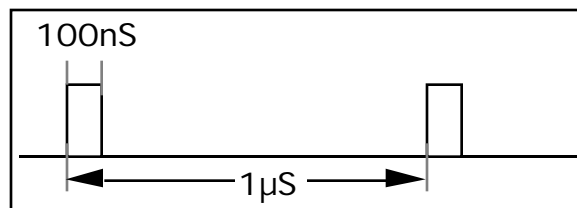


Given the input waveform shown above, design a circuit to remove the DC offset with minimal impact on the waveform.

Problem #7 10 Points

Given a 1Mhz clock, design a circuit to produce a 166.67kHz 50% duty cycle waveform.

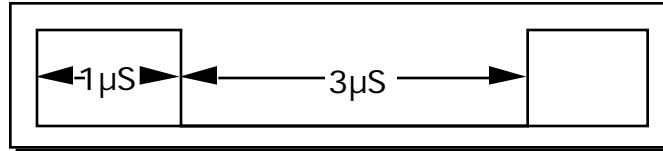
Problem #8 10 Points



Given the input signal above, design a circuit to produce the signal below.

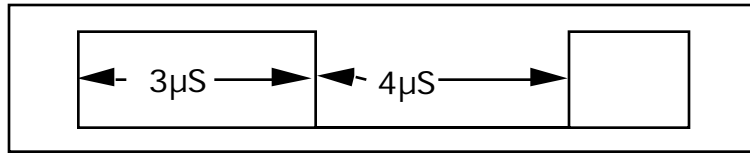
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Problem #9 10 Points

Given a 1Mhz Clock and only J-K Flip Flops and combinatorial logic, design a circuit to produce the following waveform:.



Problem #10 20 Points

Design a circuit that will respond to an input waveform with the following behavior:

- For rising edges on the input, the circuit should produce a pulse train of 10 $1\ \mu\text{s}$ (50% duty cycle, $1\ \mu\text{s}$ on - $1\ \mu\text{s}$ off) pulses.
- For falling edges on the input, the circuit should produce a pulse train of 7 $6\ \mu\text{s}$ (50% duty cycle) pulses.

You have only 1 Mhz clock and real 74LS series chips available to you. Choose real chips to implement your design. You may assume that the input waveform edges will be far enough apart so as not to casue overlap in the output waveforms. Optional: What limits does that impose on the input waveform ?

Problem #11 10 Points

Given an LED w/ $V_f=1.8\text{V}@300\text{mA}$, design a circuit, using only transistors as the active elements, to light the LED when the input to your circuit. Design your circuit so that it's input can be driven from the output of a 74LS05.