# ME218a Midterm Exam <br> Due by 4pm on 10/25/96 

Name: $\qquad$

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Include this as the cover sheet for you solutions
\#1 $\qquad$
\#2 $\qquad$
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## Midterm Examination for ME 218a

Due by $4: 00 \mathrm{pm}$ on October 25, 1996

## Problem \#1 15 Points

Given a 1Mhz Clock and only J-K Flip Flops and combinatorial logic, design a circuit to produce the following repeating waveform:.


## Problem \#2 10 Points

a) Design a Voltage Regulator using a 3.3 V Zener diode with $\mathrm{R}_{\mathrm{dyn}}=5 \Omega @ 20 \mathrm{~mA}$. It should provide between 0 and 25 mA of current into an output load. Assume an input voltage of 12 V .
b) Estimate the ripple Voltage produced if the current into the load suddenly changes from 20 mA to 22 mA .

## Problem \#3 15 Points

Your company has purchased a piece of equipment, but it does not have any indication when a measurement is being made (Poor planning, obviously not designed by someone from ME218!). Since you have had ME218, they assign you the task of adding an indicator which will light when the measurement part of the circuit is active. The only part of the circuit you can easily access will supply 1 volt and up to 1 amp when the measurement circuit is active. The power supply on the equipment, which is accessible, is rated at 10 volts and 5A. The indicator lamp that you are to use is a high intensity LED with a forward voltage drop of 1.7 volts and a maximum current that it can sustain of 50 mA . Design this circuit.

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## Problem \#4 15 Points



The Following four questions refer to the figure above. Use the following specs for the 2N2222:
$\mathrm{V}_{\mathrm{BE}(\mathrm{sat})}=0.6 \mathrm{~V}$ at $\mathrm{I}_{\mathrm{C}}=1-10 \mathrm{~mA}$ and $\mathrm{I}_{\mathrm{C}} / \mathrm{I}_{\mathrm{B}}=10$
$\mathrm{V}_{\mathrm{EBO}}=5 \mathrm{~V} \quad \mathrm{I}_{\mathrm{EBO}}=100 \mathrm{nA}$
$\mathrm{V}_{\mathrm{CBO}}=60 \mathrm{~V} \quad \mathrm{I}_{\mathrm{CBO}}=100 \mu \mathrm{~A}$
$\mathrm{V}_{\mathrm{CE}(\mathrm{SAT})}=0.25 \mathrm{~V}$ for $\mathrm{I}_{\mathrm{C}}=1-10 \mathrm{~mA}$
a) What is the output voltage if $\mathrm{V}_{\mathrm{IN}}$ is +5 Volts
b) What is the output voltage if $V_{\text {IN }}$ is -5 Volts
c) What is the base current When $\mathrm{V}_{\mathrm{IN}}$ is +12 Volts
d) What is the current in the 6.8 K resistor when $\mathrm{V}_{\text {IN }}$ is -25 Volts
e) Estimate the time constant of the rise time on the output when the output transitions from low to high. (you may ignore off state leakage currents)

## Problem \#5 10 Points

A majority voter circuit is one that takes an odd number of inputs and produces an output that reflects the majority of it's inputs.
a) Draw a truth table for a 3 bit majority voter.
b) Write the Minterm expression to describe a 3 bit majority voter.
c) Draw a Karnaugh map for the 3 bit majority voter.
d) Write the minimized expression that describes the 3 bit majority voter.
e) Design a 3 bit majority voter using standard (74xx series) Logic gates.

## Problem \#6 15 Points

For the circuit shown below, use 'Rules of Thumb' to answer the following questions:

a) What is the voltage necessary at point V2 to make the maximum current flow in the $27 \Omega$ resistor? (Assume that $\mathrm{V} 1=0 \mathrm{~V}$ )
b) Under those conditions, in which direction is the current flowing in the $27 \Omega$ resistor? How much current flow?
c) What is the voltage at point Vc under those conditions?
d) How much current must be source or sunk at point V2 to insure that all active transistors are in saturation? Indicate source/sink and magnitude.
e) How much current would flow in the $27 \Omega$ resistor if both V1 and V2 were brought to 5 V ?

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## Problem \#7 10 Points

Given a 74LS05 driving 374 C 04 inputs, design a pull-up resistor that will result in minimum power dissipation in the output stage of the 'LS05 while insuring a maximum $10-90 \%$ rise time of 50 nS . (when calculating the rise time you may ignore device leakage currents)

## Problem \#8 20 Points

You are involved in a manufacturing operation, and have been asked to design a system for monitoring the output of an assembly line.

The line can produce three types of widgets. When producing widget A , the lines produces them in groups of 3 . When producing widget B , the lines produces them in groups of 5 . When producing widget C , the lines produces them in groups of 7 . The type of widget being produced can be changed at any widget group boundary.

A sensor system is already in place that will produce a 1 mS wide TTL level pulse when a widget passes a monitoring point. When a group of widgets is passing the sensor system, the spacing between members of the group will not exceed 10 mS . The spacing between groups of widgets will be at least 100 mS . Your monitoring system should produce three outputs:

1 line that is normally low and pulses high then low for every group of widget A .
1 line that is normally low and pulses high then low for every group of widget B.
1 line that is normally low and pulses high then low for every group of widget C .
For this problem, you should use real devices that you have encountered in lectures, course readings or lab assignments. Draw a neat and readable schematic of your design and describe its operation in a narrative form.

