

ME218a Midterm Exam

Due by 4pm on 10/23/98

Name: _____

**I Certify that I have taken this examination in compliance with
the Stanford University Honor Code.**

Sign Here

Include this as the cover sheet for you solutions
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The Midterm Web Forum is at:

`http://36.37.0.17/HyperNews/get/Midterm98.html`

Other useful sites

`http://www.fairchildsemi.com/catalog/Digital.html`

`http://www.ti.com/sc/docs/as1/home.htm`

`http://mot2.mot-sps.com/logic/`

Midterm Examination for ME 218a

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Midterm Examination for ME 218a

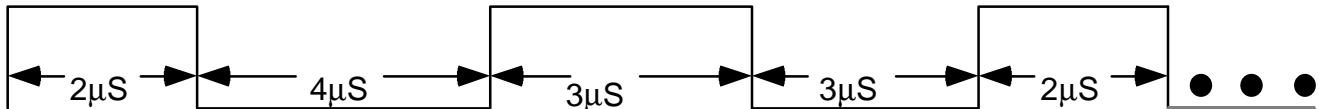
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Unless otherwise stated, the power supply for all problems is 5V.

Problem #1 15 Points



Design a circuit to produce the following repeating waveform:.



The input to your circuit should be a 1Mhz Square Wave.

Problem #2 10 Points



Given the output of a 74C04 as a control, design the necessary circuitry to power a load with a resistance of 14.5Ω and requiring at least 1A to actuate when the output of the 74C04 is high. You have a 15V supply available.

Problem #3 15 Points



You have been asked to size the pull-down resistor that will be placed on the input of a 74HC14. The pull-down resistor should guarantee a logic low input to the 74HC14 when there is nothing else connected to the 'HC14 input. From time to time, there will an 'HC14 output connected to this input, under those conditions, your pull-down resistor should not add more than $50\mu\text{A}$ to the input current required by the 'HC14.

Problem #4 15 Points



You have a signal of interest that is a sine wave at 16kHz of 1V (pk-pk) amplitude, centered at 0V. However, it is corrupted by 50Hz noise (superimposed) with an amplitude of 100mV. Design the simplest possible filter that will reduce the noise level to no more than 5mV, while introducing no more than 3% loss in the 16kHz signal. The output should also be shifted to be centered around 2.5V.

Problem #5 10 Points



Given an LTR-3208E photo transistor, design a circuit the will provide a clean logic level 0 to logic level 1 transition as the light level changes from 0 to $1\text{mW}/\text{cm}^2$ respectively. Show calculations and call out relevant specifications.

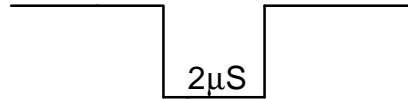
Midterm Examination for ME 218a

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Problem #6 10 Points



Design a circuit that will produce a 0.5S high pulse for every input pulse like that shown below:



These pluses will occur at random intervals, but never separated by less than 0.5S.

Problem #7 25 Points



You have been asked to design the logic for a speed regulator. The input to your circuit will be a pulse train coming from the motor that is being controlled. The goal is to control the speed of the motor such that the pulse train is at approximately 100Hz. At a constant speed, this signal will be a square wave. Your regulator circuit should produce two outputs: Accelerate and Brake. If the speed is less than 96Hz, you should activate (set high) the Accelerate line and not the Brake Line. If the speed is at or above 120Hz, you should activate (set high) the Brake line and not the Accelerate Line. If the speed is within the range, neither signal should be active. Based on the inertia of the driven system, you have been told that the command signals must be updated at least 8 times a second and that the maximum acceleration/deceleration rate is 40Hz/Sec.. From another part of the system, a highly accurate 32.768kHz square wave is available for your use. Complete your design using HC family logic devices. Be sure to label all IC pins in your schematic with their functional label, not just pin numbers.

Note: Don't get carried away with misplaced accuracy here. Take a look at the width of the acceptable speed range. Consider the impact of the conditions that you are evaluating. For instance, if you are at 96Hz and you fail to remove the accelerate signal: no big deal, you will continue to accelerate for another 1/8sec. taking you to 101Hz, where you should certainly remove the accelerate signal. **Remember:** start with blocks identifying the functions that you need.